Amendments to the Claims:

The listing of claims will replace all prior versions, and listings of claims in the applications.

Listing of Claims:

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1-12. (cancelled)

13. (currently amended) A computer system comprising:

a processor having a very large word instruction architecture and including a plurality of clusters of functional processing units, each one cluster of the plurality of clusters comprising a common number of functional processing units, the processor comprising a first prescribed number of clusters, said very large word instruction architecture allowing an instruction to have up to a second prescribed number of subinstructions, where the second prescribed number equals the first prescribed number times the common number, each instruction to be executed by the processor comprising from one subinstruction up to the second prescribed number of subinstructions, ~~along with~~ and a set of control bits, the set of control bits including a first subset of control bits equal in number to the second prescribed number, wherein the first subset of control bits identify at least one subinstruction to be shared and a routing pattern for distributing the at least one shared subinstruction; and

an instruction cache memory which stores a first VLIW instruction in a compressed format determined by a condition of the ~~set~~ first subset of control bits, the compressed format including ~~a~~ at least one shared subinstruction stored in ~~a~~ at least one given field of the first VLIW instruction, the at least one subinstruction ~~which is~~ to be shared by a plurality of the functional processing units, said plurality of functional processing units being

determined by said condition of the ~~set~~ first subset of control bits, wherein the first subset of control bits allows as many as 2^z permutations for subinstruction sharing within any given VLIW instruction, where z equals said second prescribed number.

14-22. (canceled)

23. (new) A method for processing a compressed-length VLIW instruction on a processor having a very long instruction word architecture, the compressed-length VLIW instruction including a set of control bits and at least one subinstruction, the processor comprising 'n' clusters, each one cluster of the 'n' clusters comprising a 'm' functional processing units achieving a system having 'n' times 'm' functional processing units, the set of control bits including a first subset of control bits equal in number to 'n' times 'm', wherein the first subset of control bits identify at least one subinstruction to be shared and a routing pattern for distributing the at least one shared subinstruction, the method comprising the steps of:

loading the compressed-length VLIW instruction into a cache;

testing the first subset of control bits of the compressed-length VLIW instruction to determine distribution of the at least one subinstruction, wherein each one functional processing unit of the 'n' times 'm' functional processing units receives one of a no-operation subinstruction or a subinstruction expressly included among the at least one subinstruction, wherein the first subset of control bits allows as many as 2^z permutations for subinstruction sharing within any given VLIW instruction, where z equals 'n' times 'm'.

24. (new) A method for processing a compressed-length VLIW instruction on a processor having a very long instruction word architecture, the compressed-length VLIW instruction including a set of control bits and at least one subinstruction, the processor comprising a plurality of clusters, each one cluster of the plurality of clusters comprising a plurality of functional processing units, wherein each one i^{ith} functional processing unit in a given cluster has one corresponding functional processing unit and at least one non-corresponding functional processing units in the other clusters of the plurality of clusters, the method comprising the steps of:

loading the compressed-length VLIW instruction into a cache;

testing the set of control bits of the compressed-length VLIW instruction to determine distribution of the at least one subinstruction, wherein each one functional processing unit of the plurality of functional processing units of each cluster receives one of a no-operation subinstruction or a subinstruction expressly included among the at least one subinstruction;

wherein for a first prescribed condition of the set of control bits, at least one expressly included subinstruction is routed to non-corresponding functional processing units as determined by the first prescribed condition;

wherein for a second prescribed condition of the set of control bits, at least one expressly included subinstruction is routed to multiple functional processing units as determined by the second prescribed condition, wherein the routing for the second prescribed condition is different than for the first prescribed condition; and

executing the compressed-length VLIW instruction as distributed among the plurality of functional units of each cluster by concurrently executing the subinstructions received at the plurality of functional processing units of each cluster.

25. (currently amended) A computer system comprising:

a processor having a very large word instruction architecture and including a plurality of clusters of functional processing units, each one cluster of the plurality of clusters comprising a common number of functional processing units, the processor comprising a first prescribed number of clusters; and

a memory which stores a VLIW instruction, wherein the VLIW instruction includes a set of control bits and up to a second prescribed number of subinstructions, where the second prescribed number equals the first prescribed number times the common number,

wherein the set of control bits comprises a fixed length subset of control bits which identify a routing pattern for distributing the up to the second prescribed number of subinstructions, including a designation for sharing at least one subinstruction, wherein said fixed length is the same independently of the number of subinstructions included in the VLIW instruction,

wherein each one functional processing unit of the common number of functional processing units of each cluster receives one of a no-operation subinstruction or a subinstruction expressly included among the up to the second prescribed number of subinstructions.

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